[Total No. of Questions: *12*] **[Total No. of Printed Pages:** *3*]

UNIVERSITY OF PUNE

[4362]-224

S. E. (IT) Examination - 2013

Processor Architecture & Interfacing (2008 Course)

[Time: *3* **Hours]** **[Max. Marks: 100]**

Instructions:

1 *Answer Q.1 or 2,3 or 4,and 5 or 6 from section-I and Q.7 or 8,9 or 10 and 11or 12 from section-II*

2 *Answers to the* ***two sections*** *should be written in* ***separate answer-books****.*

3 *Neat diagrams must be drawn wherever necessary.*

4 *Figures to the right indicate full marks.*

5 *Assume suitable data, if necessary.*

SECTION -I

Q.1 A Calculate physical address for the following 80386 instructions. Assume content of 80386 registers as CS=3000h, DS=4000h, SS=1000h, ES=2000h, 8

BX=2341h, DI=4563h, SI=7856h, BP=4567h

i. MOV[BP+SI+1000h],AX
ii. MOV [BX][DI], CX
iii. MOV [BP+4455h], AX
iv. MOV AX, ES:[BX]

B What is the necessity of perfetch queue? How does queue work in JUMP and CALL instruction execution? 8

OR

Q.2	A	With the help of suitable timing diagram explain Non-pipelined write bus cycle for 80386.	8
	B	State the features of 80386. Draw the real mode register set of 80386 and explain their functions.	8
Q. 3	A	Explain the following assembler directives with example. i) MODEL ii) MACRO iii) EXTRN iv) PROC	8
	B	Explain any four programming tools for assembly language program with respect to function, input, output & command	8

OR

Q. 4	A	Draw control word format of 8255 PPI and explain Mode 0 and Mode 1 (Input and output).	8
	B	Compare the following: i. DOS and BIOS ii. NEAR and FAR procedures	8
Q. 5	A	Explain the protection mechanism implemented by 80386 using privilege level checking.	12
	B	Explain the significance of following in 80386 processor. i) IOPL ii) VM iii) ET	6

OR

Q. 6	A	What is the significance of following Descriptor Table Registers? Explain with diagram. i) GDTR ii) IDTR iii) LTDR	12
	B	What is privileged instruction? Explain its significance with examples.	6

SECTION II

Q. 7	A	What is multitasking? Draw neat diagrams to explain- i) Task Register ii) Task state segment iii) TSS Descriptor	12

	B	What is the significance of debug registers? Explain DR6 & DR7.	6

OR

Q. 8	A	Compare real mode and protected mode of 80386 with respect to segmentation, interrupts processing, privilege protection and register access.	12
	B	Explain the working of confirming code segment.	6
Q. 9	A	Explain the interrupt structure of 8051 microcontroller. How does 8051 assign priority to the various interrupts?	8
	B	Explain the following SFR's of 8051- i) TCON Register ii) PCON Register	8

OR

Q. 10	A	Give significance of following pins in 8051- i) $\overline{PSEN}$ ii) $\overline{EA}$/Vpp iii) ALE iv) $\overline{INTO}$	8
	B	Explain following 8051 instructions- i) DIV AB ii)MOVC A,@A+PC iii)AJMP addr iv) RETI	8
Q. 11	A	Write 8051 algorithm to generate square wave of 2KHz frequency using Timer 1 of 8051. Assume crystal frequency of 11.0592MHz.	8
	B	State the features of PIC 16F8XX	8

OR

Q. 12	A	Explain the timer and counter operations in Mode 1 and Mode 2 of 8051.	8
	B	Explain Mode 1 and Mode 2 of serial communication in 8051 microcontroller.	8