8 May - June - 2012

Total No. of Questions—**12**] [Total No. of Printed Pages—**4**

Seat No.	

[4162]-214

S.E. (Information Technology) (Second Semester) EXAMINATION, 2012

PROCESSOR ARCHITECTURE AND INTERFACING

(2008 PATTERN)

Time : Three Hours **Maximum Marks : 100**

N.B. :— (*i*) Answer Q. No. **1** *or* Q. No. **2**, Q. No. **3** *or* Q. No. **4** and Q. No. **5** *or* Q. No. **6** from Section I and Q. No. **7** *or* Q. No. **8**, Q. No. **9** *or* Q. No. **10** and Q. No. **11** *or* Q. No. **12** from Section II.

(*ii*) Answers to the two Sections should be written in separate answer-books.

(*iii*) Neat diagrams must be drawn wherever necessary.

(*iv*) Figures to the right indicate full marks.

(*v*) Assume suitable data if necessary.

SECTION I

1. (*a*) Draw and explain non-pipelined read cycle of 80386 processor. [10]

(*b*) What is Machine Status Word (MSW) of 80386 ? Draw its format. [6]

P.T.O.

Or

2. (*a*) With the help of block diagram explain the architecture of 80386 processor. [10]

(*b*) What is the function of BE0 to BE3 signal ? Explain Memory Bank of 80386 processor. [6]

3. (*a*) What are the components of MS-DOS ? [8]

(*b*) Explain the addressing modes of 80386 showing physical address generation with example : [8]

(*i*) Direct

(*ii*) Register indirect

(*iii*) Based indexed

(*iv*) Scaled indexed with displacement.

Or

4. (*a*) Draw and explain control word format for I/O and BSR mode of 8255. [8]

(*b*) Compare and contrast : [8]

(*i*) Procedure and Macro

(*ii*) .COM and .EXE.

5. (*a*) What is DPL, RPL and CPL ? Write privilege checks performed by 80386 while accessing data or stack segment in protection mechanism. [10]

(*b*) Write down the steps to switch from RM to PM. [8]

Or

6. What is logical address, linear address and physical address in 80386 ? Explain the process by which 80386 translates logical address into physical address when paging is enabled. Explain necessary registers and memory areas used. [18]

SECTION II

7. (*a*) How does 80386 do a Task Switch ? Explain the significance and format of TSS descriptor and TSS. [10]

(*b*) What is Virtual mode ? How to switch from protected mode to virtual 86 mode ? [6]

Or

8. (*a*) What is Call Gate ? Explain how call gate can be used to call a function with a higher privilege level. [8]

(*b*) What is Interrupt Gate Descriptor ? Explain the process of interrupt handling in protected mode with the help of IDT and IDTR. [8]

9. (*a*) Explain the physical structure and significance of all the I/O ports of the 8051 microcontroller. [8]

(*b*) Explain interrupt structure of 8051 microcontroller with their priority structure. [6]

(*c*) Explain IP register format and program IP register to assign the highest priority to INT1. [4]

Or

10. (*a*) Design and draw a 8051 based microcontroller system with the following specifications. Also draw memory map for given memory devices : [10]

(*i*) 8051 working at 12 MHz frequency.

(*ii*) 32 kB program memory.

(*iii*) 32 kB data memory.

(*b*) Draw and explain internal memory organization of 8051 microcontroller. [8]

11. (*a*) Write a program that continuously gets 8 bit data from P0 and send it to P1 while simultaneously creating a square wave of 200 microseconds period on pin P2.1. Use timer 0 interrupt with mode 2 to create the square wave. Assume crystal frequency = 11.0592 MHz. [10]

(*b*) List the features of PIC 16F8XX. [6]

Or

12. (*a*) Explain any *two* operating modes of Timer of 8051. [8]

(*b*) Explain SCON, SBUF and PCON special function registers and their utility. [8]